PATENT ABSTRACTS OF JAPAN

(11) Publication number: (43) Date of publication of application: 25.01.2002

2002-025950

(51)Int.Cl. H01L 21/304 B24B 7/17

B24B 37/04

(21)Application number: 2000-199561 (71)Applicant: MITSUBISHI MATERIALS SILICON

CORP

(22)Date of filing: 30.06.2000 (72)Inventor: MATAGAWA SATOSHI MORITA ETSURO

(54) MANUFACTURING METHOD FOR SEMICONDUCTOR WAFER (57) Abstract:

PROBLEM TO BE SOLVED: To provide a

manufacturing method of the semiconductor wafer with small amount of surface abrasion and small time thereof while keeping the specular state of the rear face and making identification of the front and rear faces possible.

SOLUTION: After layout, a lapped silicon wafer is subjected to alkali-etching, and the surface of the etched wafer is abraded with an abrading amount of about 10 μ m and a damage of 1 to 3 μ m. The specular finishing of the front face and the slight grinding for the uneven rear face of the wafer with the front face grinding amount of about 7 μ m and the rear face grinding amount of 1.5 μ m or below. The rear face is not made completely specular, so a sensor can identify the front and rear. At that time, the rough unevenness of the rear face can be prevented, and the contamination stuck to the rear face can be prevented.

The inflection of the rear face caused by alkali etching can be prevented, transcription of the inflection to the specular face can be prevented, and a decrease in resolution of exposition in a following step can be prevented. At the same time nano-topography can be prevented through the concurrent grinding, and a decrease in yield caused by a worse distribution of film thickness in a CMP step can be prevented.

* NOTICES *

JPO and INPIT are not responsible for any damages caused by the use of this translation.

- 1. This document has been translated by computer. So the translation may not reflect the original precisely.
- 2,**** shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1]A manufacturing method of a semiconductor wafer characterized by comprising the following.

An alkali dirty process of etching a semiconductor wafer after a lap with an alkaline etching reagent.

Then, a surface grinding operation which uses a grinding stone for low damages and grinds a low damage on the surface of a semiconductor wafer.

Then, a double-sided polishing process which grinds lightly unevenness formed in a rear face of a semiconductor water in an alkali dirty process at the same time it carries out mirror polishing of the surface of a semiconductor wafer.

[Claim 2]A manufacturing method of the semiconductor wafer according to claim 1 whose polishing quantity of the rear face the amount of surface lapping of a semiconductor wafer in the above-mentioned double-sided polishing process is 0.5-1.5 micrometers in 3-10 micrometers.

[Translation done.]

* NOTICES *

JPO and INPIT are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

100011

Field of the Invention]This invention relates to the manufacturing method of a semiconductor wafer, and the manufacturing method of the semiconductor wafer which has little polishing quantity and in which polishing time is short while high flatness and nano topography can obtain the semiconductor wafer of smallness in detail.

100001

[Description of the Prior Art]In manufacture of a silicon wafer, after slicing an ingot and producing a silicon wafer, to this silicon wafer, each process of camfering, wrapping, acid dirty, and mirror polishing is given one by one. In the acid dirty process, the wafer just behind a lap was immersed in mixed acid, and distortion by the lap processing, distortion by a camfering process, etc. are removed. It has the advantage that reactivity with this acid dirty ** and a silicon wafer is high, and an etch rate is quick. At acid dirty ** and one side, it is generated by a lot of air bubbles during etching, and the wave of the cycle of about 10 mm, ten height - about 100 nm of numbers occurs to rear surface both sides of a wafer under the influence. As a result, the display flatness or nano topography of the wafer surface was falling. [0003] By the way, in the photolithography process in a device process, if a silicon wafer is adsorbed at a wafer retainer board, the phenomenon in which the wave on the rear face of a wafer is transferred by the wafer surface by which mirror polishing was carried out will occur. Thereby, the resolution of exposure fell and the yield of the device was small. Then, the "manufacturing method of the semiconductor wafer" shown, for example in the patent No. 2910507 gazette is known as a conventional method which suppresses such a transfer phenomenon. This conventional method changed etching of the RAPPUDO wafer into the alkali etching which used the alkaline etching reagent from the acid etching till then. And in from this alkali dirty process before the mirror-polishing process of a wafer surface, the unevenness formed in the wafer rear face of alkali etching is ground lightly, and the ****** polish process of decreasing the width of that unevenness is included, thus, acid -- each inconvenience which the wave generated at the time of acid dirty was canceled, and was mentioned above as a result by replacing with dirtily and adopting ARUKARIETCHI will be canceled. [0004]the "double-sided grinding method of the semiconductor wafer" of the statement is known by JP,11-233462,A, for example as art in which a wafer surface produces from the former the one side mirror surface wafer (rear-face half mirror surface wafer) from which a part of unevenness on the back was removed in the mirror plane. In order to change the grinding rate on a wafer surface and the rear face of a wafer in this conventional technology, While adopting abrasive cloth with small holding power of a slurry, and polishing speed slow as abrasive cloth which grinds a wafer rear face, abrasive cloth with large holding power of a slurry and polishing speed guick as abrasive cloth of a wafer surface was adopted. [0005]

Problem(s) to be Solved by the Invention]However, the following technical problems had occurred in such conventional technologies. namely, the former alkall — if it depends dirtily, although canceled, to rear surface both sides of a silicon wafer, every direction is a size which is 10-20 micrometers, and unevenness of about 2 micrometers of differences of elevation will

appear fear of wave generating, in order [for this reason,] to mirror-plane-ize a wafer surface in a subsequent mirror-polishing process -- alkali -- unevenness of the wafer surface depended dirtily must be removed at the time of mirror polishing. The polishing tune was long, [0006] in the conventional silicon wafer by which acid dirty processing was carried out, when double-sided polish was given, the wafer rear facewas [mirror-plane-] easy to beized. Since the granularity appeared at the time of acid dirty is only about about only 1 micrometer only in the height even if this changes the polishing speed of the wafer surface by the abrasive cloth for wafer surfaces, and the polishing speed on the rear face of a wafer by the abrasive cloth for wafer rear faces, it is because it will be shaved off easily. [0007]

[Objects of the Invention]This invention is high flatness, and there is little polishing quantity of a wafer, and its polishing time is short, and it sets it as that purpose that a wafer rear face moreover provides the manufacturing method of the semiconductor wafer whichis [mirror-plane-] hard to beized at the time of double-sided polish of a wafer. This invention can detect a wafer rear face with a photosensor, and sets it as that purpose to provide the manufacturing method of the semiconductor wafer which can distinguish the rear surface of a wafer.

Means for Solving the Problem]An alkali dirty process that the invention according to claim 1 etches a semiconductor wafer after a lap with an alkaline etching reagent, A surface grinding operation which uses a grinding stone for low damages for the surface of a semiconductor wafer, and grinds a low damage after this alkali dirty, after performing this surface grinding, at the same time it carries out mirror polishing of the surface of a semiconductor wafer -- alkali -- it is a manufacturing method of a semiconductor wafer provided with a double-sided polishing process which grinds lightly unevenness therefore dirtily formed in a rear face of a semiconductor wafer.

[0009]As a semiconductor wafer, a silicon wafer can be mentioned, for example. As an alkaline etching reagent, solutions, such as KOH and NaOH, are mentioned, for example. Ecthing quantity in this case is 15 in all-30 micrometers of wafer rear surface both sides. And in a surface grinding operation, surface grinding of a low damage is performed at the time of the finishing, combination of primary surface grinding only with good finishing surface grinding my which is carried out and is ground comparatively coarsely, and finishing surface grinding may be sufficient. It may finish with primary surface grinding and secondary grinding and 3rd grinding may be performed between surface grinding.

[0010]A grinding amount of this surface grinding is 3-15 micrometers. As a grinding stone built into surface grinding attachment for finishing, a resinoid grinding wheel is employable, for example. It is more desirable for there not to be a wafer surface easily and to use a grinding stone of the high yarn count which can moreover be ground also in respect of a non-damage in this finishing surface grinding operation. If an example is given — #1000-#8000 - 1 it is a resinoid grinding wheel of #2000 - #4000 preferably. As a more concrete grinding stone for finishing surface grinding, a resinoid grinding wheel of #1500 by disco incorporated company - #3000, etc. are mentioned, for example. 'IF-01-1-4 / 6-B-M01" (trade name of a grinding stone) are especially preferred. A vitrified grinding wheel of #300 - #600 can be used for primary surface grinding.

[0011]A working damage after surface grinding is 1-3 micrometers, for example. If a damage is senious, polishing quantity of a wafer surface in next double-sided polish will increase. When this polishing quantity exceeds 10 micrometers, there is a possibility that exaggerated polish of the rear face may be carried out, and it may pose a problem that polishing time becomes long in a perfect mirror plane. In this invention, since a low damage is ground to a wafer surface before carrying out simultaneous polish of wafer rear surface both sides, polishing quantity of a wafer surface can be reduced to less than (for example, about 7 micrometers) 10 micrometers. Therefore, polishing time is shortened and a throughput improves. Perfect mirror plane-ization by exaggerated polish on the back can be prevented.

[0012] Polishing quantity of a wafer surface in the above-mentioned double-sided polishing

process is not limited. Usually, it becomes smaller [the conventional polishing quantity] than 12 micrometers. For example, it is 7 micrometers. A hard urethane foam pad, a pad which made a nonwoven fabric impregnate with and harden urethane resin, etc. are mentioned to abrasive cloth used, for example.

[0013]wafer rear-face polish of this double-sided polishing process — alkali — unevenness therefore dirtily formed in a rear face of a semiconductor wafer is ground slightly, a part of that unevenness is removed, and it means making this wafer rear face into a half-mirror plane. Polishing quantity on a rear face of a wafer is usually about 0.5-1.5 micrometers. As abrasive cloth, each abrasive cloth for the above-mentioned wafer surfaces is employable. A method of carrying out half-mirror surface finish of the wafer rear face is not limited at the same time it mirror-plane-izes a wafer surface. For example, a method of changing polishing speed of a wafer surface by abrasive cloth for wafer surfaces and polishing speed on a rear face of a wafer surface. Such constitution of the wafer rear faces etc. may be used. As a double-sided polishing process, LPD-300 by Fujikoshi machinery incorporated company (device name), etc. is mentioned, for example.

[0014]The invention according to claim 2 is a manufacturing method of the semiconductor wafer according to claim 1 whose polishing quantity of a rear face of a semiconductor wafer the amount of surface lapping of a semiconductor wafer in the above-mentioned double-sided polishing process is 3-10 micrometers, and is 0.5-1.5 micrometers. Inconvenience that a damage remains on the surface in less than 3 micrometers in the amount of surface polishes arises. If it exceeds 10 micrometers, polishing time will become long and a throughput will fall. [0015]At less than 0.5 micrometer, a rear-face granularity reduction effect runs short of polishing quantity on a rear face of a wafer. If it exceeds 1.5 micrometers, inconvenience that discernment of a rear surface by mirror-plane-izing is impossible will arise. Thus, based on luminosity (degree of brilliancy) of a wafer surface and rear surface, a surface and rear race of a wafer surface was polishing quantity on 3-10 micrometers and a rear face of a wafer shall be polishing quantity of a wafer surface 0.5-1.5 micrometers and a

[Function] According to this invention, alkali dirty [of the RAPPUDO wafer] is carried out, and surface grinding of a low damage is carried out to a wafer surface. The polishing quantity of next double-sided polish. Since the polishing quantity by this surface grinding at the time of next double-sided polish. Since the polishing quantity in polish of the wafer surface where a grinding damage is small is set to less than 10 micrometers, polishing quantity becomes less and polishing time is shortened. After surface grinding, a wafer rear face is lightly ground at the same time it carries out mirror polishing of the wafer surface. As a result, coarse unevenness does not occur at the wafer rear face. The rear-face discernment by subsequent device processes becomes easy. Generating of a NANOTOPO gley is also cancelable.

[Both] [Embodiment of the Invention]Hereafter, the example of this invention is described with reference to drawings. <u>Drawing 1</u> is a flow plan which shows the manufacturing method of the semiconductor wafer concerning one example of this invention. <u>Drawing 2</u> is an explanatory view of the double-sided polish device used for the manufacturing method of the semiconductor wafer concerning one example of this invention. <u>Drawing 3</u> is an important section expanded sectional view of this double-sided polish device. If it is in this example as shown in <u>drawing 1</u>, a semiconductor wafer is produced through each process of a slice, camfering, a lap, alkali dirty, surface grinding, double-sided polish, and finishing washing. Hereafter, each process is explained in detail.

[0018]The silicon ingot which was able to be pulled up by the CZ process is a slice step (S101), and is sliced by the 8-inch silicon wafer about 860 micrometers thick. Next, camfering (S102) is performed to this silicon wafer. That is, the peripheral part of a wafer cuts off the corners coarsely in predetermined shape with the grinding stone for metal camfering of #600. Thereby, the peripheral part of this wafer is fabricated by the shape (for example, MOS type chamfered shape) which is tinged with a predetermined radius of circle.

[0019]Next, the silicon wafer in which this chamfering work was performed is wrapped by a

lapping process (\$103). In this lapping process, a silicon wafer is arranged between the lap surface plates mutually kept parallel, and the lap liquid which is a mixture of an alumina abrasive grain, a dispersing agent, and water is slushed between this lap surface plate and silicon wafer. And the lap of wafer rear surface both sides is mechanically carried out by performing rotation and adjustment under application of pressure. The lap amount in this case is about 40 in all-80 micrometers about rear surface both sides of a wafer.

[0020]Then, alkali etching is performed to the silicon wafer after this lapping process (\$104). A high-concentration NaOH solution is used as an alkaline etching reagent. The etching temperature is 90 ** and etching time is 6 minutes. The etching quantity at this time is about 20 micrometers in all of wafer rear surface both sides. Thus, since it replaced with the conventional acid etching and lakali etching was adopted, in wafer rear surface both sides, the wave of the cycle of about 10 mm, ten height - 100 mm of numbers does not occur. [0021]Next, a surface grinding operation is given to this etched wafer (\$105). Specifically, surface grinding is given by the surface grinding attachment which carries a #2000 No. resinoid grinding wheel. The grinding amount at this time is about 10 micrometers. The working damage after surface drinding is 1-3 micrometers.

[0022]Double-sided polish which performs simultaneously light polish of the mirror finish of the surface of a silicon wafer and unevenness on the rear face of a wafer is given after this surface grinding (S106). As this double-sided polish device, the double-sided polish device shown in drawing 2 and drawing 3 is adopted. Hereafter, this double-sided polish device is explained briefly. In drawing 2 and drawing 3, 10 is a double-sided polish device, in this double-sided polish device 10, the silicon wafer W is inserted and held in the wafer holding hole 12 formed in the carrier plate 11, and both sides of each wafer W are ground simultaneously, supplying the slurry which contains polished abrasive from that upper part to the silicon wafer W. I two or more 1 [0023]Namely, between the solar gear 13 and the internal gear 14 which were provided enabling free rotation, The carrier plate 11 which has the outside gear 11a is formed in a peripheral part, enabling rotation and free revolution, Both sides of the silicon wafer W are simultaneously ground by pressing and ****ing rear surface both sides (a top, the undersurface) of the silicon wafer W are simultaneously ground the abrasive cloth 15 and the abrasive cloth 15 and the abrasive cloth 15 and the

100.24)The abrasive cloth by Rodel Nitta CO. with which the holding power of a slurry is large and the polishing speed of a wafer surface becomes quick as the abrasive cloth 15 which grinds the surface (mirror plane) of the silicon wafer W (a part for 0.5-micrometer/), for example, "suba800", is adopted, a wafer rear face (half-mirror plane) — the abrasive cloth by Rodel Nitta CO. "UR-100" with which the holding power of a slurry is small and the polishing speed on the rear face of a wafer becomes slow as abrasive cloth of business (a part for 0.07-micrometer/) is adopted. Thus, since the abrasive cloth of a different raw material in which a difference arises at the holding power of a slurry in the abrasive cloth 15 for wafer surfaces and the abrasive cloth 16 for wafer rear faces, and a difference is given to polishing speed was adopted, At the time of double-sided polish of a wafer, as for a wafer rear face, mirror finish ***-**are [mirror-plane-] also hard tolze a wafer surface. The polishing quantity of the wafer surface by this double-sided polish is about 7 micrometers. On the other hand, the polishing quantity on the rear face of a wafer is 1.5 micrometers or less.

[0025] Thus, low damage grinding is beforehand given to the wafer surface by which mirror polishing is carried out with the surface grinding operation. Therefore, in this double-sided polishing process, the polishing quantity of that wafer surface can be reduced to 7 micrometers. Thus, since polishing quantity decreases, polishing time is shortened. By being lightly ground at the time of this double-sided polish, the wafer rear face can remove a part of coarse unevenness generated at the wafer rear face at the time of alkali dirty, and can stop the degree of this unevenness.

[0026]And since the polishing quantity at the time of rear-face polish was 0.5-1.5 micrometers, luminosity on the rear face of a wafer can be made into the luminosity which can detect a wafer rear surface here using a wafer rear-face detection sensor. Therefore, a wafer surface and a

wafer rear face are automatically discriminable. Then, this silicon wafer is made and a washing process (\$107) is given. Specifically, it is considered as washing of an RCA system. [0027]

[Effect of the Invention]According to this invention, ARUKARIETCHI is given to a RAPPUDO wafer

Then, since the wafer rear face was lightly ground in the polishing process, it can suppress that coarse unevenness appears at the wafer rear face, and adhesion of the garbage to a rear face can be reduced.

And since a wafer rear face is not formed into a perfect mirror plane even if it performs doublesided polish of a wafer, it becomes detectable [the wafer rear surface by a sensor]. Since surface grinding of the low damage is given beforehand, the polishing quantity of a wafer surface can be reduced in the wafer surface by which mirror polishing is carried out, and the throughput in a polishing process improves to it. alkali -- dirty -- more -- a wave on the back -- deterring generating -- the wave to a mirror plane -- it can prevent the resolution of exposure by a device process falling by having prevented transfer. The nano topography occurrence prevention by double-sided simultaneous polish can protect device yield lowering, such as thickness distribution agoravation by a CMP process.

[Translation done.]